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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/609,312	06/24/2003	Kenneth W. Marr	303.859US1	8022

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EXAMINER	
SIDDIQUI, SAQIB JAVAID	

ART UNIT	PAPER NUMBER
2117	

MAIL DATE	DELIVERY MODE
04/23/2007	PAPER

Please find below and/or attached an Office communication concerning this application or proceeding.

Advisory Action Before the Filing of an Appeal Brief	**Application No.** 10/609,312	**Applicant(s)** MARR, KENNETH W.	
	Examiner Saqib J. Siddiqui	**Art Unit** 2117	

--The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

THE REPLY FILED 29 March 2007 FAILS TO PLACE THIS APPLICATION IN CONDITION FOR ALLOWANCE.

1. ☐ The reply was filed after a final rejection, but prior to or on the same day as filing a Notice of Appeal. To avoid abandonment of this application, applicant must timely file one of the following replies: (1) an amendment, affidavit, or other evidence, which places the application in condition for allowance; (2) a Notice of Appeal (with appeal fee) in compliance with 37 CFR 41.31; or (3) a Request for Continued Examination (RCE) in compliance with 37 CFR 1.114. The reply must be filed within one of the following time periods:
   a) ☐ The period for reply expires _____ months from the mailing date of the final rejection.
   b) ☒ The period for reply expires on: (1) the mailing date of this Advisory Action, or (2) the date set forth in the final rejection, whichever is later. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of the final rejection.

   Examiner Note: If box 1 is checked, check either box (a) or (b). ONLY CHECK BOX (b) WHEN THE FIRST REPLY WAS FILED WITHIN TWO MONTHS OF THE FINAL REJECTION. See MPEP 706.07(f).

Extensions of time may be obtained under 37 CFR 1.136(a). The date on which the petition under 37 CFR 1.136(a) and the appropriate extension fee have been filed is the date for purposes of determining the period of extension and the corresponding amount of the fee. The appropriate extension fee under 37 CFR 1.17(a) is calculated from: (1) the expiration date of the shortened statutory period for reply originally set in the final Office action; or (2) as set forth in (b) above, if checked. Any reply received by the Office later than three months after the mailing date of the final rejection, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

NOTICE OF APPEAL

2. ☐ The Notice of Appeal was filed on _____. A brief in compliance with 37 CFR 41.37 must be filed within two months of the date of filing the Notice of Appeal (37 CFR 41.37(a)), or any extension thereof (37 CFR 41.37(e)), to avoid dismissal of the appeal. Since a Notice of Appeal has been filed, any reply must be filed within the time period set forth in 37 CFR 41.37(a).

AMENDMENTS

3. ☐ The proposed amendment(s) filed after a final rejection, but prior to the date of filing a brief, will not be entered because
   (a) ☐ They raise new issues that would require further consideration and/or search (see NOTE below);
   (b) ☐ They raise the issue of new matter (see NOTE below);
   (c) ☐ They are not deemed to place the application in better form for appeal by materially reducing or simplifying the issues for appeal; and/or
   (d) ☐ They present additional claims without canceling a corresponding number of finally rejected claims.

   NOTE: _____. (See 37 CFR 1.116 and 41.33(a)).
4. ☐ The amendments are not in compliance with 37 CFR 1.121. See attached Notice of Non-Compliant Amendment (PTOL-324).
5. ☐ Applicant's reply has overcome the following rejection(s): _____.
6. ☐ Newly proposed or amended claim(s) _____ would be allowable if submitted in a separate, timely filed amendment canceling the non-allowable claim(s).
7. ☒ For purposes of appeal, the proposed amendment(s): a) ☐ will not be entered, or b) ☒ will be entered and an explanation of how the new or amended claims would be rejected is provided below or appended.

   The status of the claim(s) is (or will be) as follows:
   Claim(s) allowed: _____.
   Claim(s) objected to: _____.
   Claim(s) rejected: *13-16,48-65 and 76-78*.
   Claim(s) withdrawn from consideration: _____.

AFFIDAVIT OR OTHER EVIDENCE

8. ☐ The affidavit or other evidence filed after a final action, but before or on the date of filing a Notice of Appeal will not be entered because applicant failed to provide a showing of good and sufficient reasons why the affidavit or other evidence is necessary and was not earlier presented. See 37 CFR 1.116(e).
9. ☐ The affidavit or other evidence filed after the date of filing a Notice of Appeal, but prior to the date of filing a brief, will not be entered because the affidavit or other evidence failed to overcome all rejections under appeal and/or appellant fails to provide a showing a good and sufficient reasons why it is necessary and was not earlier presented. See 37 CFR 41.33(d)(1).
10. ☐ The affidavit or other evidence is entered. An explanation of the status of the claims after entry is below or attached.

REQUEST FOR RECONSIDERATION/OTHER

11. ☒ The request for reconsideration has been considered but does NOT place the application in condition for allowance because: See Continuation Sheet.
12. ☐ Note the attached Information Disclosure Statement(s). (PTO/SB/08) Paper No(s). _____
13. ☐ Other: _____.

GUY LAMARRE
PRIMARY EXAMINER

Continuation of 11. does NOT place the application in condition for allowance because: Applicant contends that prior art of record Namekawa US Pat no. 6,115,301 does not teach a first supply node, a second supply node and the switching units. The Examiner respectfully disagrees. Applicant does not define in the claim limitations, whether the supply node is with respect to a certain memory segment on the device. Therefore, given the broadest possible interpretation, under one interpretation first supply node is Figure 1 # 80, where Vcc is being provided to the defective memory cell arrays and supply node second is Figure 1 # 10, where voltage is being applied to the capacitors, transistors and word lines.

With respect to the switching circuits, Namekawa teaches "The switches constituting the first and second switch circuit groups 50 and 60 are controlled by the decode circuits D0, . . . , D15 constituting a decoder group 70, respectively. More specifically, the non-inverted output terminal of the decode circuit D0 is connected to the switch SW20, and the inverted output terminal is connected to the switch SW10. The non-inverted output terminal of the decode circuit D1 is connected to the switch SW21, and the inverted output terminal is connected to the switch SW11. In the same manner as described above, the non-inverted output terminal of the decode circuit D15 is connected to the switch SW215, and the inverted output terminal is connected to the switch SW115. The output terminal of a defective address memory circuit 80 is connected to the input terminals of the decode circuits D0, . . . , D15. The defective address memory circuit 80 stores the address of a defective data line, and stores data representing whether the data line is replaced. The defective address memory circuit 80 outputs, depending on an input column or row address, the address of a defective data line constituted by a signal of a plurality of bits and a signal representing whether a data line is replaced. The decode circuits D0, . . . , D15 generally turn on the respective switches of the first switch circuit group 50 depending on an output signal from the defective address memory circuit 80, and turn off the switches of the second switch circuit group 60. On the other hand, when data lines are to be replaced, depending on an output an output signal from the defective address memory circuit 80, output signals from decode circuits corresponding to a defective data line and a redundant data line and an output signal from a decode circuit located between these decode circuits are inverted. For example, the data line DL4 has a defect, output signals from the decode circuits D0, . . . , D4 are simultaneously inverted depending on the output signal from the defective address memory circuit 80. The switches SW10, . . SW14 of the first switch circuit group 50 are turned off, and the switches SW20, . . . , SW24 of the second switch circuit group 60 are turned on. For this reason, the data line DL4 is replaced with the data line DL3, and the data line DL3 is replaced with the data line DL2. In the same manner as described above, the data line DL0 is replaced with the redundant data line RDL. The replacing operations by the switches are simultaneously performed depending on the output signals from the decode circuits D0, . . . , D4." (Figure 1, column 6, lines 5-55).

It is clear from Figure 1 that the switches are connected in series with the memory segments with respect to the internal nodes in the memory cell array and the second supply nodes, which are the switches as in order for a switch to be working there needs to be node to supply voltage. When the defective address memory (Figure 1 # 80) sends a select signal to the Decoders, they turn the respective switch off to electrically disconnect the memory cell array from the respective supply node (switch). The respective decoders act as a supply control circuit by isolating the memory segment using the switches.

Examiner did take Official Notice, but Examiner believes that the switching circuitry in Namekawa does teach the claimed limitations, however since the reference does not explicitly go into the details of the working of the switching circuitry Examiner chose to give an obviousness rejection. Further, evidence of the Official Notice is provided in US Pat no. 5,416,740 (column 8, lines 30-45), where when a defective memory cell is detected the switching circuitry cuts of the power from the memory cells by blowing a fuse.

Lastly, Examiner would like to assert that the peak of obviousness is anticipation therefore the obviousness rejections are maintained even though Namekawa anticipates on all the claimed limitation.